We Accelerate Connectivity

1-64G-112G ePHY™ Multi-Protocol SerDes IP: Ultra Low Latency, Low Power

Overview

eTopus designs ultra-high speed mixed-signal semiconductor IP solutions for high-performance computing and data center applications. Our 1-64G-112Gbps multi=protocol ultra-high speed SerDes IP is adopted by global Tier-1 network/storage/5G OEMs and major semiconductor companies.

eTopus is the pioneer on PAM4 ADC/DSP-based SerDes, the first startup demonstrated 56Gbps PAM4 in 2016. The system architecture has been proven and enhanced for 3 generations to 112Gbps PAM4 in 7 and 6 nm. This IP is optimized for low power (<5pj/bit) and latency < 5ns.

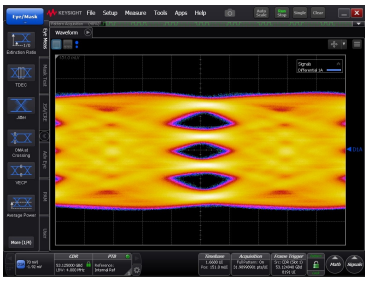
Our unique and patented DSP algorithms provide excellent scalability to support short reach optical channel to long reach copper like backplane and DAC cables with superior Bit Error Rates (BER) and extremely robust Clock Data Recovery (CDR) as featured in International Solid State Circuits Conference (ISSCC 2021).

This is a multi-protocol SERDES supporting PCIe Gen 6, PCIe Gen 5, CXL2 and latest ethernet protocols.

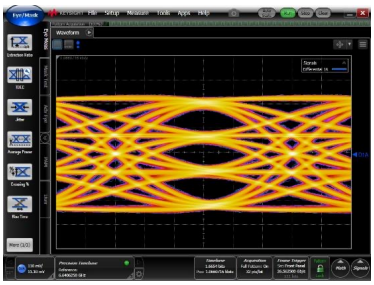
Benefits

- Robust Clock Data Recovery, never-lose-lock™ even at 1e-2 BER channel condition
- Superior post-Forward Error Correction Bit Error Rate with minimum error propagation.
- Extremely stable system performance with fast temperature tracking
- Easy SoC integration with auto system tuning through proprietary HW/SW algorithms
- Scalable short to long reach performance with low power < 5pj/bit consumption and suitable for Ultra Low Latency applications <5nS latency.

ePHY™ Transmit Eye



106.25 Gbps



53.125 Gbps

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Product Highlights

- Multi-protocol ePHY IP supports 1-64G-112Gbps data ratesLatest PCIe Gen 6 and below supported
- Low-Jitter Transmitter with 8-tap de-emphasis FIR filter
- Adaptive receive equalizer scales from short to long reach (45dB+)
- On-chip real-time monitor for channel quality and receive eye measurement
- Upgradable firmware for post-silicon extensible functionality
- Support IEEE802.3bj/cd, InfiniBand EDR, and OIF CEI-25G-LR/MR/SR/VSR Electrical Interfaces

ePHY IP Features

01 On-chip AC-coupled receiver eliminates on-board decoupling capacitors

02 Dual power supply rails further reduce system BOM cost

03 Low jitter full chip clock distribution architecture

04 Quad/Octal/Hex configurations per PLL with tight lane skew control

05 Integrated common PLL for quad/octa/hexl configuration minimizes power consumption

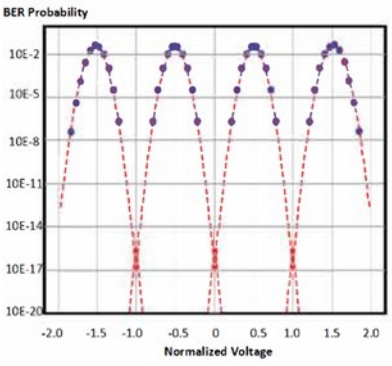
06 Layout supports north/south and east/west (escape routings and package stack-up guidelines provided)

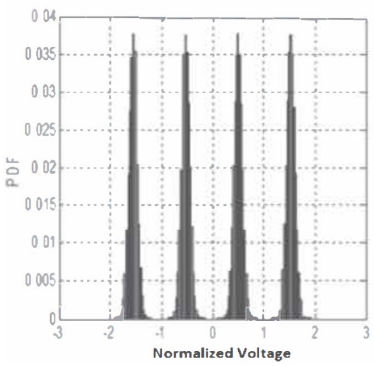
07 Comprehensive BIST supporting PRBS testing of major standards

08 Pseudo Reed-Solomon Forward Error Correction (RSFEC) error analyzer provides multi-bit error analysis

09 Receive impulse response measurement for in-situ end-application system integration

BER Bathtub Plot ePHY





IP Deliverables

System Deliverables

- Software Development Kit
- Reference Board
- IBIS AMI Model
- CPM Power Model

Frontend Deliverables

- Verilog Behavioral Model
- Timing Libraries

Backend Deliverables

- LEF
- GDS
- CDL
- DRC & LVS reports

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