We Accelerate Connectivity

PCI Express GEN5 EP / RC/ DM Integrated with Multi-Protocol Serdes

Overview

PCIE Gen 1-5 is a layered protocol high speed interconnect interface supporting speeds up to 32GT/S and multi lanes and links. The layers specified in PCIe specification Transport, Datalink, Physical layers (digital packet) are implemented in IP along with optimized serdes interface logic connecting to eTopus 56G and 112G multi-protocol ynm Serdes PHY and AXI Bridging logic to connect to applications.

eTopus designs ultra-high speed mixed-signal semiconductor IP solutions for high-performance computing and data center applications. Our 1-64G-112Gbps multi-protocol ultra-high speed SerDes IP is adopted by global Tier-1 network/storage/5G OEMs and major semiconductor companies.

eTopus is the pioneer on PAM4 ADC/DSP-based SerDes, the first startup demonstrated 56Gbps PAM4 in 2016. The system architecture has been proven and enhanced for 3 generations to 112Gbps PAM4 in 7 and 6 nm. This IP is optimized for low power (<6pj/bit) and latency < 5ns.

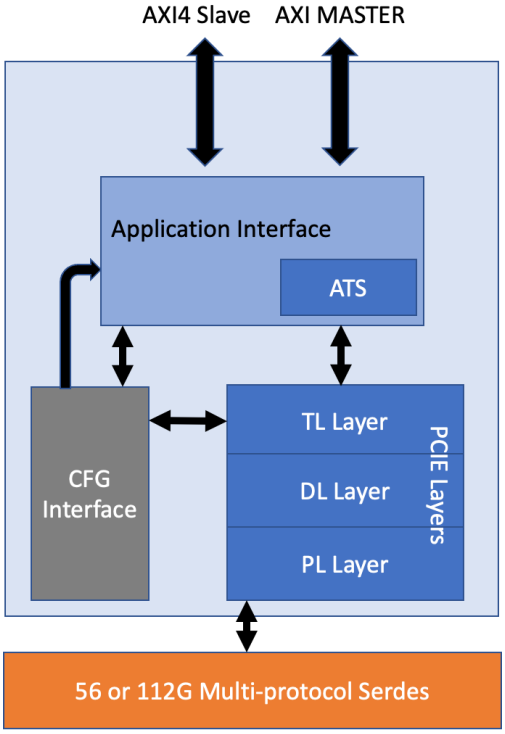
Our patented DSP algorithms provide excellent scalability to support short reach optical channel to long reach copper like backplane and DAC cables with superior Bit Error Rates (BER) and extremely robust Clock Data Recovery (CDR).

The PCI Express Gen 5 supports End point, Root Complex and Dual Mode Operation & is bundled with 56G 7nm SERDES IP & 112G 7nm SERDES IP. For chiplets and high speed applications a low latency version is available.

Features

- Compliant with PCI Express 5.0, 4.0 and Previous Versions
- (32 GT/s), (16 GT/s), (8GT/s), (5 GT/s), (2.5 GT/s)
- Compliant with Pipe 5.X
- Supports both Pipe SerDes architecture
- EP/RC/DM configurations supported
- Compliant with ATS specification
- Compliant with AMBA interfaces
- 512b architecture and 32/64B Pipe interface for lower latency
- Compliant with SR-IOV specification
- Supports X16, X8, X4, X2, XI lanes
- Highly configurable, robust DMA architecture
- Flexible user interface & AXI4/Native intefaces
- LTR, AER, OBFF, MSI, MSI-X, PTM, ARI, ECRC and all features supported
- Simple clocking architecture
- 32 Physical and 512 virtual functions supported
- Optional in built address translator configurable
- FPGA validation @Gen5 speed and loopback mode
- Support 1G and 2G clocking for lowest latency

Block Diagram



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Status

Status	: Silicon in Progress	Simulation	: Verilog, Cadence, Xsim
Availability	: Immediate	FPGA	: Only for Validation
Language	: Verilog, System Verilog	Technology	: 7/6 nm
Synthesis	: TBD	PD Flows	: Available

Specification

Configurable Options

- Maximum link width (x1, x2, x4, x8, x16)
- MPS (128B to 4KB)
- MRRS (128B to 4KB)
- Transmit retry/receive buffer size
- Number of virtual channels
- L1 PM substate support
- Optional capability features can be configured
- Number of PF/VF
- DMA configurable options
- AXI MAX payload size variations

Design Attributes

- Highly modular and configurable design
- layered architecture
- Fully synchronous design
- Simple clock domain architecture
- software control for major functionalities
- Debug options
- Safety feature handling
- DFT friendly design
- Optimized for Low Latency
- 1G & 2G clocking supported

Deliverables

Product Package

- Verilog RTL code
- UVM based testbench and behavioral models
- test cases
- Protocol checkers and performance cases
- Synthesis Scripts

Documentation

- Design datasheet
- Verification guide
- Synthesis guide

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